

We Claim:

1. A method of writing to cache comprising:
 - initiating a write operation to a cache;
 - in a first operational mode:
 - detecting the presence or absence of a write miss;
 - if a write miss is absent, writing data to said cache;
 - if a write miss is present, retrieving said data from a further memory and writing said data to said cache;
 - in a second operational mode:
 - placing said cache in a memory mode;
 - writing said data to said cache regardless of whether a write miss is present or absent.
2. The method of claim 1 wherein:
 - said second operational mode is designated by a memory mode bit.
3. The method of claim 2 wherein:
 - said memory mode bit is stored in a device control register.
4. The method of claim 1 wherein:
 - said initiating a write operation includes specifying an address;
 - said second operational mode is designated by address bits contained within said address.

5. The method of claim 4 wherein:

said by address bits contained within said address include the high order address bits equaling 1111.

6. The method of claim 1 wherein:

said initiating a write operation includes specifying an address;
said second operational mode includes retrieving a bin identifier from said address, said bin identifier designating a compartment of said cache where said data is to be written.

7. The method of claim 1 wherein:

said second operational mode includes setting a select all bins bit to invalidates cache directory entries associated with writing said data.

8. A system of writing to cache comprising:

a cache directory;

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a cache array;

control logic for writing a valid field and an address to said cache directory and data to said cache array, said control logic including:

hit miss complex logic for determining a compartment of said cache directory and said cache array to be updated upon detecting a cache hit in a first operation mode;

least recently used (LRU) complex logic for determining a compartment of said cache directory and said cache array to be updated upon detecting a cache miss in said first operational mode;

said control logic determining a compartment of said cache directory and said cache array to be updated regardless of a cache hit or cache miss in a second operational mode.

9. The system of claim 8 wherein:

said second operational mode is designated by a memory mode bit.

10. The system of claim 9 further comprising:

a device control register storing said memory mode bit.

11. The system of claim 8 wherein:

said second operational mode is designated by address bits contained within said address.

12. The system of claim 11 wherein:

 said by address bits contained within said address include the high order address bits equaling 1111.

13. The system of claim 8 wherein:

 said control logic retrieves a bin identifier from said address, said bin identifier designating said compartment of said cache where said data is to be written.

14. The system of claim 8 wherein:

 said control logic invalidates cache directory entries associated with writing said data in response to a select all bins bit.